



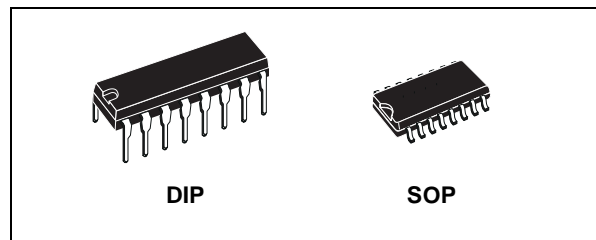
# HCF4076B

## 4 BIT D TYPE REGISTERS

- THREE STATE OUTPUTS
- INPUT DISABLE WITHOUT GATING THE CLOCK
- GATED OUTPUT CONTROL LINES FOR ENABLING OR DISABLING THE OUTPUTS
- BUFFERED INPUTS AND OUTPUTS
- QUIESCENT CURRENT SPECIFIED UP TO 20V
- 5V, 10V AND 15V PARAMETRIC RATINGS
- INPUT LEAKAGE CURRENT  
 $I_l = 100\text{nA (MAX) AT } V_{DD} = 18\text{V } T_A = 25^\circ\text{C}$
- 100% TESTED FOR QUIESCENT CURRENT
- MEETS ALL REQUIREMENTS OF JEDEC JESD13B "STANDARD SPECIFICATIONS FOR DESCRIPTION OF B SERIES CMOS DEVICES"

### DESCRIPTION

HCF4076B is a monolithic integrated circuit fabricated in Metal Oxide Semiconductor technology available in DIP and SOP packages. HCF4076B is a four bit register consisting of D-TYPE flip-flops that feature three state outputs. Data Disable inputs are provided to control the entry of data into the flip-flops. When both Data

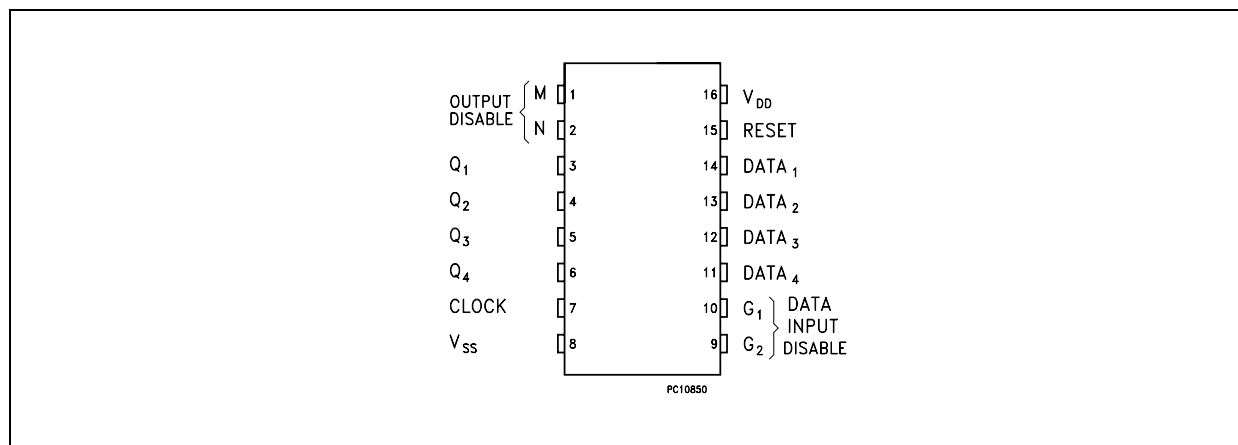


### ORDER CODES

PACKAGE	TUBE	T & R
DIP	HCF4076BEY	
SOP	HCF4076BM1	HCF4076M013TR

Disable inputs are low, data at the D inputs are loaded into their respective flip-flops on the next positive transition of the clock input. Output Disable inputs are also provided. When the Output Disable inputs are both low, the normal logic states of the four outputs are available to the load. The outputs are disabled independently of the clock by a high logic level at either Output Disable input, and present a high impedance.

### PIN CONNECTION



**IINPUT EQUIVALENT CIRCUIT**



**PIN DESCRIPTION**

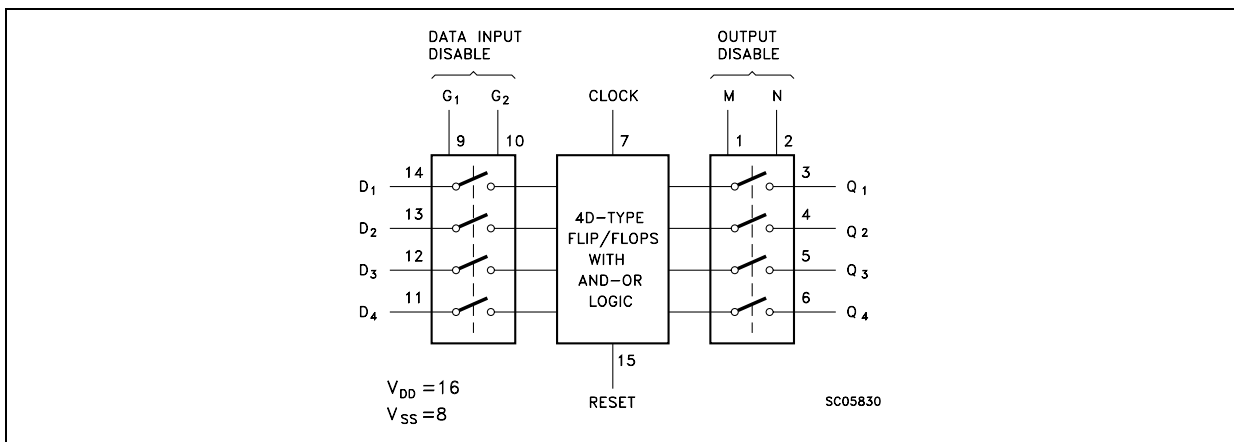
PIN No	SYMBOL	NAME AND FUNCTION
14, 13, 12, 11	DATA1 to DATA 4	D Inputs
10, 9	G1, G2	Data Input Disable Control
1, 2	M, N	Output Disable Control
7	CLOCK	Clock Input
15	RESET	Reset Input
8	V <sub>SS</sub>	Negative Supply Voltage
16	V <sub>DD</sub>	Positive Supply Voltage

**TRUTH TABLE**

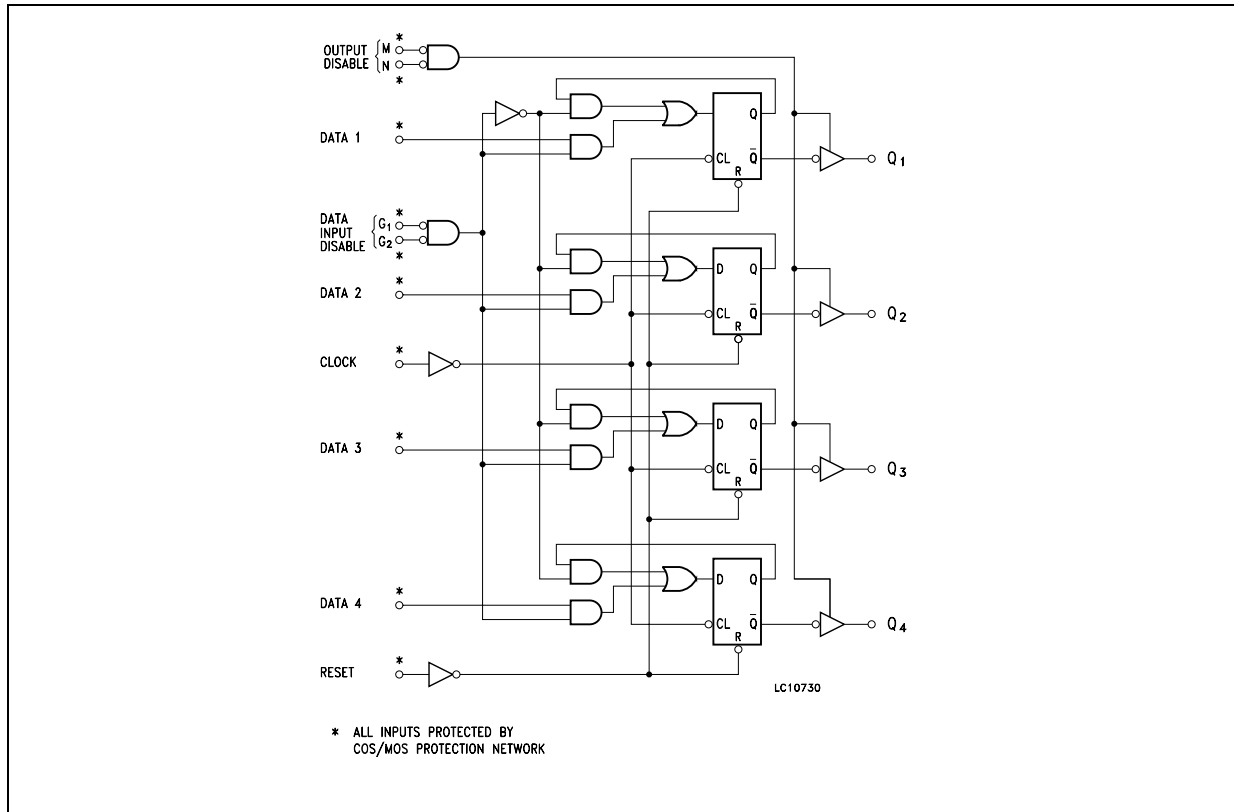
RESET	CLOCK	DATA INPUT DISABLE		DATA D	NEXT STATE OUTPUT	
		G1	G2			
H	X	X	X	X	L	
L	L	X	X	X	Q	NO CHANGE
L		H	X	X	Q	NO CHANGE
L		X	H	X	Q	NO CHANGE
L		L	L	H	H	
L		L	L	L	L	
L	H	X	X	X	Q	NO CHANGE
L		X	X	X	Q	NO CHANGE

X : Don't Care  
 When either Output Disable M or N is high, the outputs are disabled (high impedance state) : however sequential operation of the flip-flop is not affected.

**FUNCTIONAL DIAGRAM**



**LOGIC DIAGRAM**



**ABSOLUTE MAXIMUM RATINGS**

Symbol	Parameter	Value	Unit
$V_{DD}$	Supply Voltage	-0.5 to +22	V
$V_I$	DC Input Voltage	-0.5 to $V_{DD} + 0.5$	V
$I_I$	DC Input Current	$\pm 10$	mA
$P_D$	Power Dissipation per Package	200	mW
	Power Dissipation per Output Transistor	100	mW
$T_{op}$	Operating Temperature	-55 to +125	$^{\circ}C$
$T_{stg}$	Storage Temperature	-65 to +150	$^{\circ}C$

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied.

All voltage values are referred to  $V_{SS}$  pin voltage.

**RECOMMENDED OPERATING CONDITIONS**

Symbol	Parameter	Value	Unit
$V_{DD}$	Supply Voltage	3 to 20	V
$V_I$	Input Voltage	0 to $V_{DD}$	V
$T_{op}$	Operating Temperature	-55 to 125	$^{\circ}C$

## DC SPECIFICATIONS

Symbol	Parameter	Test Condition				Value						Unit	
		V <sub>I</sub> (V)	V <sub>O</sub> (V)	I <sub>OL</sub>   ( $\mu$ A)	V <sub>DD</sub> (V)	T <sub>A</sub> = 25°C			-40 to 85°C		-55 to 125°C		
						Min.	Typ.	Max.	Min.	Max.	Min.		Max.
I <sub>L</sub>	Quiescent Current	0/5			5		0.04	5		150		150	$\mu$ A
		0/10			10		0.04	10		300		300	
		0/15			15		0.04	20		600		600	
		0/20			20		0.08	100		3000		3000	
V <sub>OH</sub>	High Level Output Voltage	0/5		<1	5	4.95			4.95		4.95		V
		0/10		<1	10	9.95			9.95		9.95		
		0/15		<1	15	14.95			14.95		14.95		
V <sub>OL</sub>	Low Level Output Voltage	5/0		<1	5		0.05			0.05		0.05	V
		10/0		<1	10		0.05			0.05		0.05	
		15/0		<1	15		0.05			0.05		0.05	
V <sub>IH</sub>	High Level Input Voltage		0.5/4.5	<1	5	3.5			3.5		3.5		V
			1/9	<1	10	7			7		7		
			1.5/13.5	<1	15	11			11		11		
V <sub>IL</sub>	Low Level Input Voltage		4.5/0.5	<1	5			1.5		1.5		1.5	V
			9/1	<1	10			3		3		3	
			13.5/1.5	<1	15			4		4		4	
I <sub>OH</sub>	Output Drive Current	0/5	2.5	<1	5	-1.36	-3.2		-1.1		-1.1		mA
		0/5	4.6	<1	5	-0.44	-1		-0.36		-0.36		
		0/10	9.5	<1	10	-1.1	-2.6		-0.9		-0.9		
		0/15	13.5	<1	15	-3.0	-6.8		-2.4		-2.4		
I <sub>OL</sub>	Output Sink Current	0/5	0.4	<1	5	0.44	1		0.36		0.36		mA
		0/10	0.5	<1	10	1.1	2.6		0.9		0.9		
		0/15	1.5	<1	15	3.0	6.8		2.4		2.4		
I <sub>I</sub>	Input Leakage Current	0/18	Any Input		18		$\pm 10^{-5}$	$\pm 0.1$		$\pm 1$		$\pm 1$	$\mu$ A
I <sub>OZ</sub>	3-State Output Current	0/18	Any Input		18		$\pm 10^{-4}$	$\pm 0.4$		$\pm 12$		$\pm 12$	$\mu$ A
C <sub>I</sub>	Input Capacitance		Any Input				5	7.5					pF

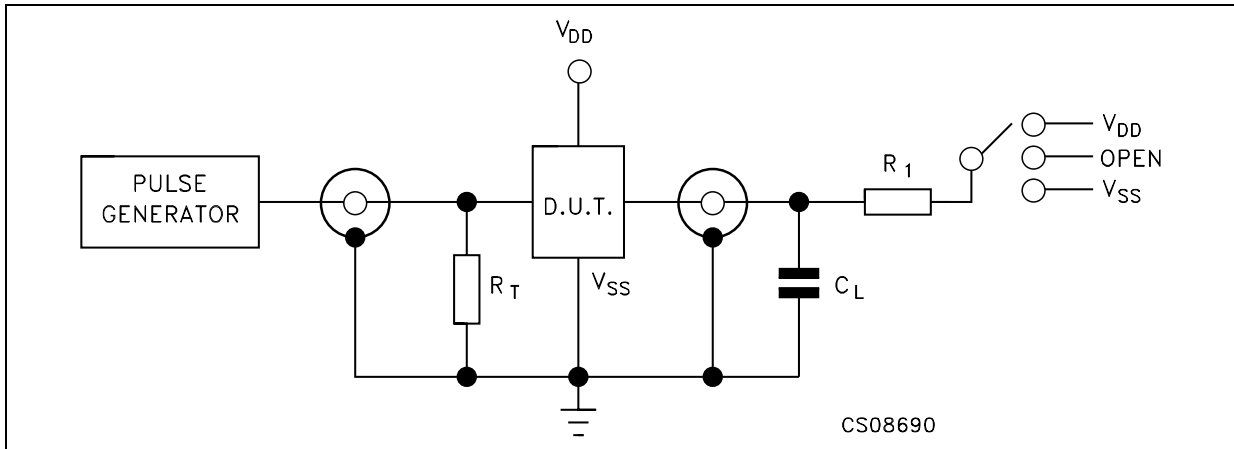
The Noise Margin for both "1" and "0" level is: 1V min. with V<sub>DD</sub>=5V, 2V min. with V<sub>DD</sub>=10V, 2.5V min. with V<sub>DD</sub>=15V

**DYNAMIC ELECTRICAL CHARACTERISTICS** ( $T_{amb} = 25^{\circ}\text{C}$ ,  $C_L = 50\text{pF}$ ,  $R_L = 200\text{K}\Omega$ ,  $t_r = t_f = 20\text{ ns}$ )

Symbol	Parameter	Test Condition		Value (*)			Unit
		$V_{DD}$ (V)		Min.	Typ.	Max.	
$t_{PLH}$ $t_{PHL}$	Propagation Delay Time (Clock to Q Output)	5			300	600	ns
		10			125	250	
		15			90	180	
$t_{PHL(R)}$	Propagation Delay Time (Reset)	5			230	460	ns
		10			100	200	
		15			75	150	
$t_{P(1-H)}$	3-State Out H or L to High Impedance	5	$R_L = 1\text{K}\Omega$		150	300	ns
		10			75	150	
		15			60	120	
$t_{P(L-1)}$	3-State High Impedance to H or L Output	5	$R_L = 1\text{K}\Omega$		150	300	ns
		10			75	150	
		15			60	120	
$t_W$	Clock Pulse Width	5		200	100		ns
		10		100	50		
		15		80	40		
$t_W$	Reset Pulse Width	5		120	60		ns
		10		50	25		
		15		40	20		
$t_{setup}$	Data Setup Time	5		200	100		ns
		10		80	40		
		15		60	30		
$t_{setup}$	Data Input Disable Setup Time	5		180	90		ns
		10		100	50		
		15		70	35		
$f_{max}$	Maximum Clock Frequency	5		3	6		MHz
		10		6	12		
		15		8	16		
$t_r$ , $t_f$	Clock input Rise or Fall Time	5		15			$\mu\text{s}$
		10		5			
		15		5			

 (\*) Typical temperature coefficient for all  $V_{DD}$  value is 0.3 %/°C.

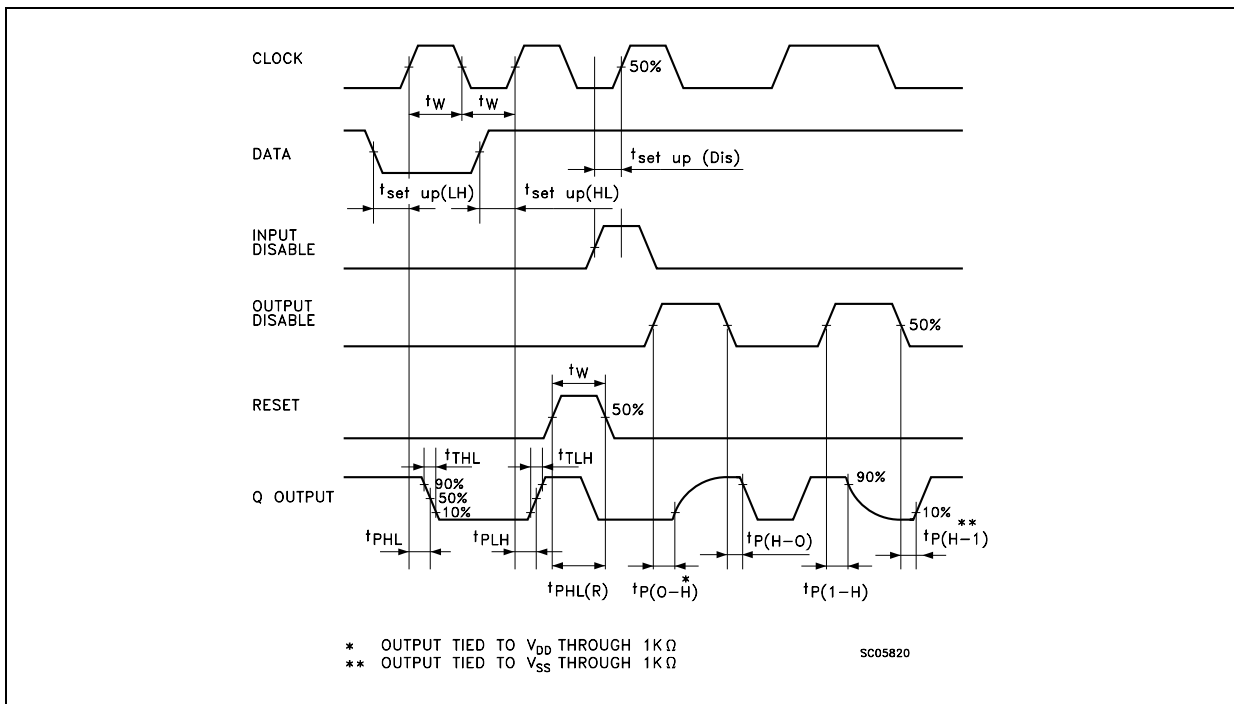
TEST CIRCUIT



TEST	SWITCH
$t_{PLH}$ , $t_{PHL}$	Open
$t_{PZL}$ , $t_{PLZ}$	$V_{DD}$
$t_{PZH}$ , $t_{PHZ}$	$V_{SS}$

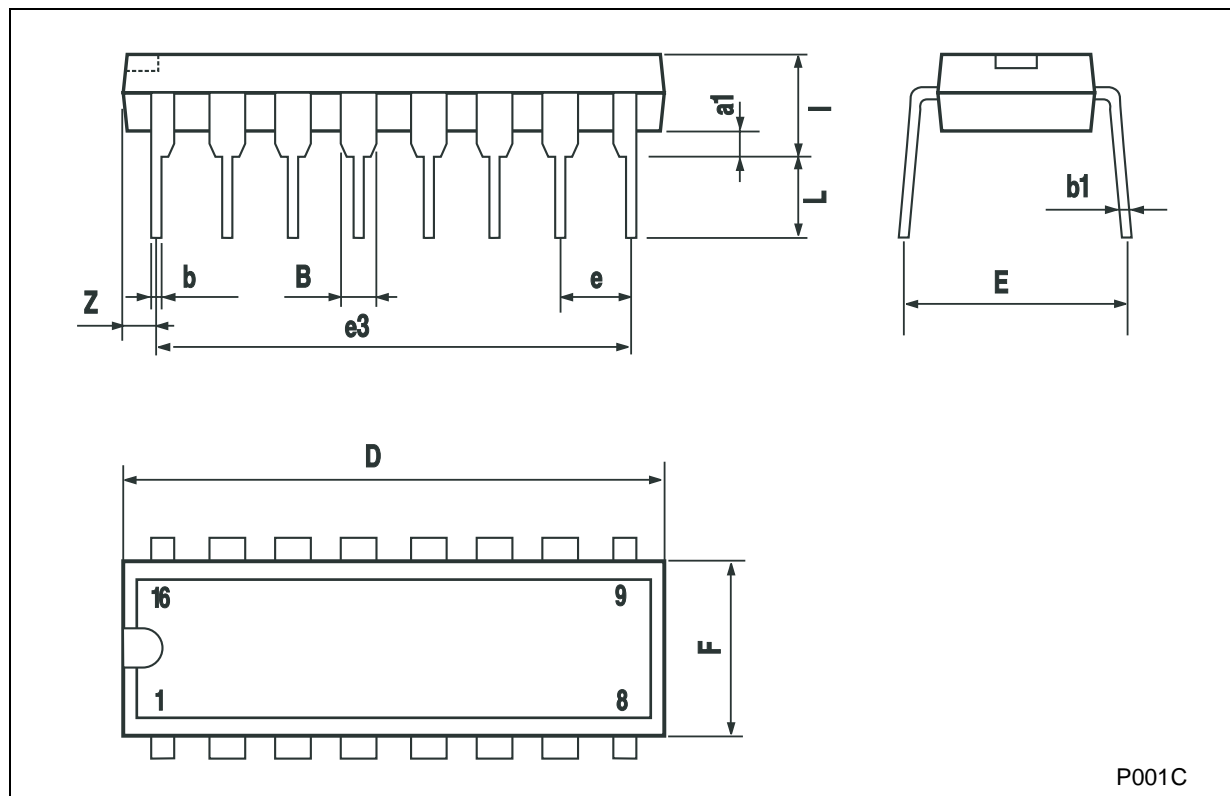
$C_L = 50\text{pF}$  or equivalent (includes jig and probe capacitance)  
 $R_L = 200\text{K}\Omega$   
 $R_T = Z_{OUT}$  of pulse generator (typically  $50\Omega$ )

WAVEFORM : PROPAGATION DELAY TIMES ( $f=1\text{MHz}$ ; 50% duty cycle)



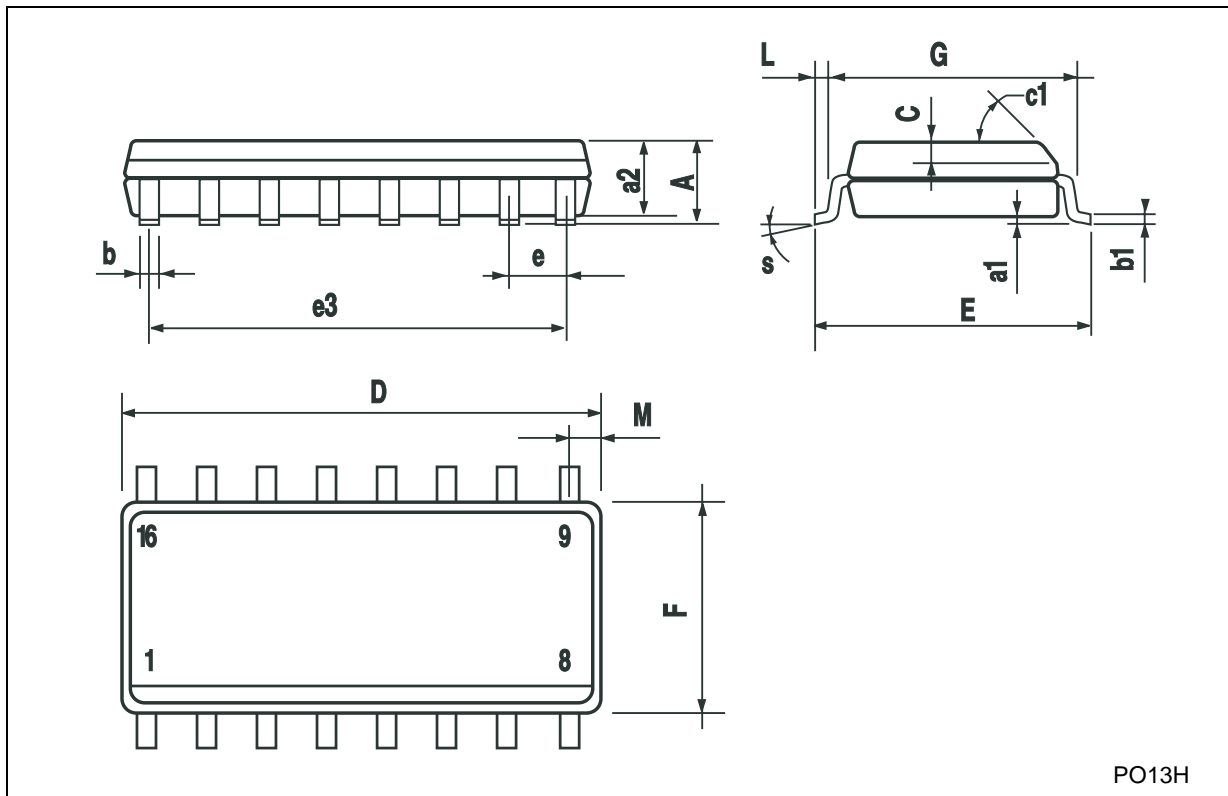
### Plastic DIP-16 (0.25) MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
a1	0.51			0.020		
B	0.77		1.65	0.030		0.065
b		0.5			0.020	
b1		0.25			0.010	
D			20			0.787
E		8.5			0.335	
e		2.54			0.100	
e3		17.78			0.700	
F			7.1			0.280
I			5.1			0.201
L		3.3			0.130	
Z			1.27			0.050



**SO-16 MECHANICAL DATA**

DIM.	mm.			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.75			0.068
a1	0.1		0.2	0.003		0.007
a2			1.65			0.064
b	0.35		0.46	0.013		0.018
b1	0.19		0.25	0.007		0.010
C		0.5			0.019	
c1	45° (typ.)					
D	9.8		10	0.385		0.393
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		8.89			0.350	
F	3.8		4.0	0.149		0.157
G	4.6		5.3	0.181		0.208
L	0.5		1.27	0.019		0.050
M			0.62			0.024
S	8° (max.)					



PO13H



Information furnished is believed to be accurate and reliable. However, STMicroelectronics assumes no responsibility for the consequences of use of such information nor for any infringement of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of STMicroelectronics. Specifications mentioned in this publication are subject to change without notice. This publication supersedes and replaces all information previously supplied. STMicroelectronics products are not authorized for use as critical components in life support devices or systems without express written approval of STMicroelectronics.

© The ST logo is a registered trademark of STMicroelectronics

© 2002 STMicroelectronics - Printed in Italy - All Rights Reserved  
STMicroelectronics GROUP OF COMPANIES

Australia - Brazil - Canada - China - Finland - France - Germany - Hong Kong - India - Israel - Italy - Japan - Malaysia - Malta - Morocco  
Singapore - Spain - Sweden - Switzerland - United Kingdom - United States.

© <http://www.st.com>

